



TSMS-01-1440C

SW

May 11, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/822,197 04/09/04

Kuo-Chi Tu et al.

METHOD OF FABRICATING AN EMBEDDED
DRAM FOR METAL-INSULATOR-METAL
(MIM) CAPACITOR STRUCTURE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on May 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 5/17/04

TSMC-01-1440C

U.S. Patent 6,211,061 to Chen et al., "Dual Damascene Process for Carbon-Based Low-K Materials," teaches a dual damascene process with carbon-based low-k materials.

The following three U.S. Patents discuss MIM capacitor processes:

- 1) U.S. Patent 6,096,597 to Tsue et al., "Method for Fabricating an Integrated Circuit Structure."
- 2) U.S. Patent 6,329,234 to Ma et al., "Copper Process Compatible CMOS Metal-Insulator-Metal Capacitor Structure and Its Process Flow."
- 3) U.S. Patent 6,271,084 to Tu et al., "Method of Fabricating a Metal-Insulator-Metal (MIM) Capacitor Structure Using a Damascene Process."

Sincerely,

A handwritten signature in black ink, appearing to read "SBA", with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

